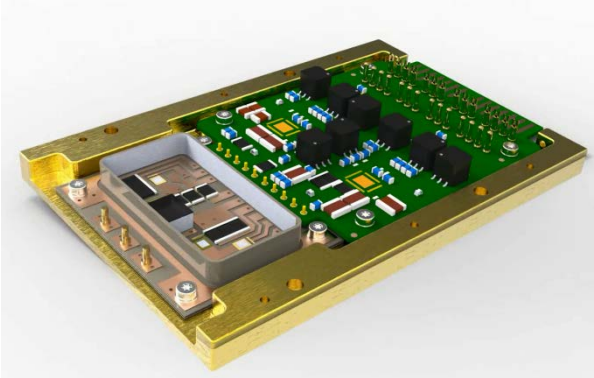
Half Bridge SiC BJT & SJT Driver

DRIV Series

FEATURES

- Half Bridge device
- Temperature range -55°c to +230°C
- Isolated data transmission through multi-channel transceiver
- Half bridge cross-conduction protection
- Under Voltage Protection
- Drain desaturation detection
- Gate Failure detection
- Over current protection

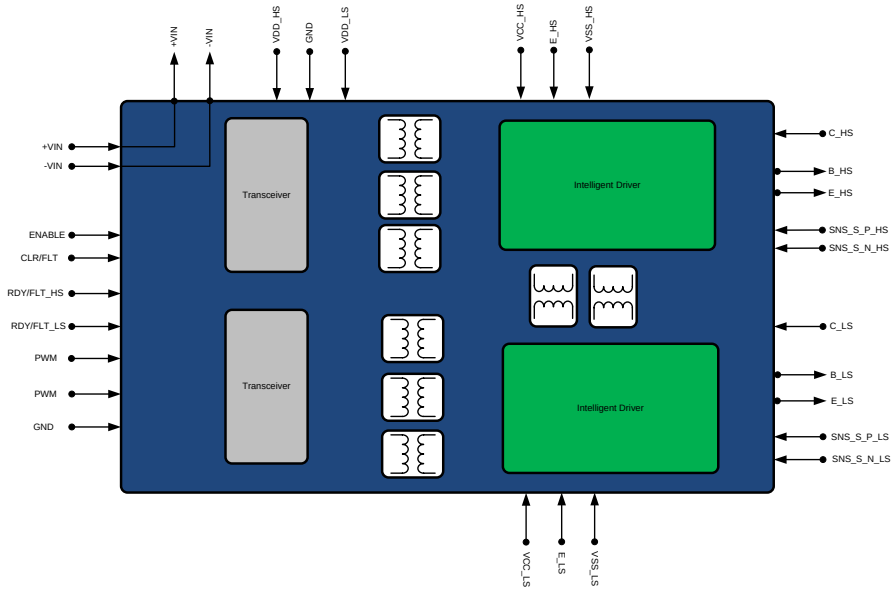


APPLICATIONS

- Half Bridge Driver for 1.2kV, SiC BJT & SJT Modules
- Intelligent Power Modules (IPM)
- DC/DC converters and switched mode power supplies (SMPS)
- Harsh environment such as aeronautic, oil & gas, electrical traction and many others

SPECIFICATIONS

BLOCK DIAGRAM



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PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	+VIN	
2	-VIN	
3	ENABLE	Digital input transmitter enable pin to be connected to **VDD** to enable transmition
4	CLR/FLT	Input receiving the CLEAR/FAULT information from the micro-controller. This signal can be use like a reset of both driver stage
5	RDY/FLT_HS	Output giving the READY/FAULT information of the high side driver to the micro-controller through the isolated transceiver
6	RDY/FLT_LS	Output giving the READY/FAULT information of the low side driver to the micro-controller through the isolated transceiver
7	PWM	Input receiving the PWM signal from the micro-controller
8	GND	Negative power supply supplying the transceiver stage. This potential is common of both transceiver
9	VCC_HS	Positive supply voltage of the high side driver
11	VSS_HS	Most negative supply voltage of the high side driver
12	VDD_HS	Positive power supply supplying high side transceiver stage
13	VDD_LS	Positive power supply supplying low side transceiver stage
14	VCC_LS	Positive supply voltage of the low side driver
16	VSS_LS	Most negative supply voltage of the low side driver
17	C_HS	Sense node through external resistor divider of the **COLLECTOR** terminal of the high side power switch for desaturation detection.
18	B_HS	Output of the high side driver, connected to the **BASE** terminal of the high side power switch
19	E_HS	Connected to the **EMITTER** terminal of the high side power switch
20	SNS_S_P_HS	Positive sense pin of the **EMITTER** terminal of the high side power switch source (over-current detection). Connect it to the **EMITTER** of the high side switching device, on the top of the sense resistor, using a Kelvin electrical connection. If the sense current feature is not required, this pin must be shorted with **SNS_S_N_HS** and connected to **E_HS** potential.
21	SNS_S_N_HS	Negative sense pin of the **EMITTER** terminal of the high side power transistor (over-current detection). Connect it to the bottom of the emitteur sense resistor using a Kelvin electrical connection. If the sense current feature is not required, this pin must be shorted with **SNS_S_P_HS** and connected to **E_HS** potential.
22	C_LS	Sense node through external resistor divider of the **COLLECTOR** terminal of the high side power switch for desaturation detection.
23	B_LS	Output of the high side driver, connected to the **BASE** terminal of the low side power switch
24	E_LS	Connected to the **EMITTER** terminal of the low side power switch
25	SNS_S_P_LS	Positive sense pin of the **EMITTER** terminal of the low side power switch source (over-current detection). Connect it to the **EMITTER** of the high side switching device, on the top of the sense resistor, using a Kelvin electrical connection. If the sense current feature is not required, this pin must be shorted with **SNS_S_N_LS** and connected to **E_LS** potential.
26	SNS_S_N_LS	Negative sense pin of the **EMITTER** terminal of the low side power transistor (over-current detection). Connect it to the bottom of the emitteur sense resistor using a Kelvin electrical connection. If the sense current feature is not required, this pin must be shorted with **SNS_S_P_LS** and connected to **E_LS** potential.

ELECTRICAL PARAMETERS

HALF BRIDGE DRIVER - ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Drivers Power Supply Voltage VCC-VSS	Driver only	7		40	V
Transceiver Power Supply Voltage VDD	Transceiver only	-0.5		5.5	V
Output peak Current			6		A
Output average curent			0.5		A
Max. Switching frequency	Duty cycle 50%	10		100	kHz
Input to output isolation			1500		V
High side to low side isolation	AC 60s		1500		V
Transient Common mode immunity			20		kV/µs
Operating temperature		-55		+230	°c
Storage temperature		-55		+230	°c

TRANSCEIVER - ELECTRICAL CHARACTERISTICS Tcase=25°C otherwise specified

PARAMETER	DESIGNATION	CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Power supply		4.5	5	5.5	V
Iio	Quiescent current	Input = “0” output =”0”		100		µA
Isc	Supply current	Nomial functionnement		20		mA
VIH	Digital inputs		3.84			V
VIL	Digital inputs				1.1	V
	Hysteresis		1.6	2	2.4	V
VOH	Digital outputs	Iout=8mA	4.4			V
VOL	Digital Outputs	Iout=8mA			0.63	V

DRIVER POWER SUPPLY

PARAMETER	DESIGNATION	CONDITIONS	MIN	TYP	MAX	UNIT
VCC-E	Positive power supply		5.25	5.5	5.75	V
E-VSS	Negative Power supply		6	7	30	V
	Quiescent current consumption			25		mA
	UVLO	VCC-VSS		11.2		V
	UVLO	E-VSS		5.1		V

FAILURE DETECTION

PARAMETER	DESIGNATION	CONDITIONS	MIN	TYP	MAX	UNIT
Drain desaturation	Internal comparator reference vs. VSS		0.45	0.55	0.65	V
	Allowed input current on SNS_D pin	When clamping at about 1.4V vs. VSS		5		mA
	SNS_D leakage current	0.45V≤VSNS_D≤0.65V			500	nA
Gate's short circuit	Gate current threshold			3		A
	Gate current threshold accuracy			20		%
Overcurent power module	Emitter shunt voltage threshold			100		mV
	Emitter shunt voltage threshold accuracy			20		%

DRIVER DEVICE

DESIGNATION	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay	From PWM to driver output		650		ns
Rise time	1nF output capacitor		TBD		
Fall time	1nF output capacitor		TBD		
Dead time	Cross-conduction protection active		430		ns
ON Peak output current	100nF output capacitor (VCC=5.5V)		TBD		A
Continuous output current			450	mA	
Soft-shutdown transistor R_{ON}		50	100	150	Ω

CONTROL

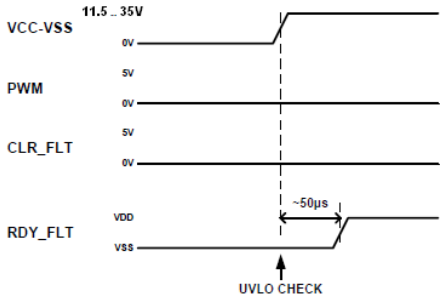
DESIGNATION	MIN	TYP	MAX	UNIT
Blanking time		1		µs
Blanking time accuracy		20		%
Miller Clamp delay		220		ns
Miller Clamp delay accuracy		20		%
Pulse width ON		220		ns
Pulse width ON accuracy		20		%

OPERATION PHASE

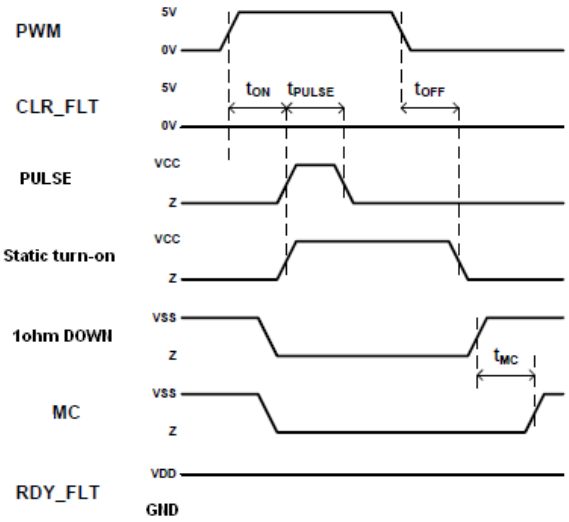
The operations describes below are for one stage driver. These operations are running in the same time for the both stage driver.

Startup Phase

The startup phase is initialized by the turn on of the power supplies of the circuit VCC-VSS and VDD. The UVLOs are checked and if the power supplies values are higher than the fixed thresholds and the output **BASE** is close to VSS, an internal counter with a delay of 50µs is started. This delay secures the correct turn-on of the internal voltage reference. During the startup phase the input PWM is blanked (If a PWM signal is received, it is not transferred to the driver outputs). At the end of the counter the signal RDY/FLT goes to "1". The circuit enters into the functional phase: if a PWM signal is received, it is transferred to the driver outputs.



Functional phase



The functional phase starts when the RDY_FLT output flags a "1". In this phase, the circuit is ready to receive the PWM signal from the microcontroller.

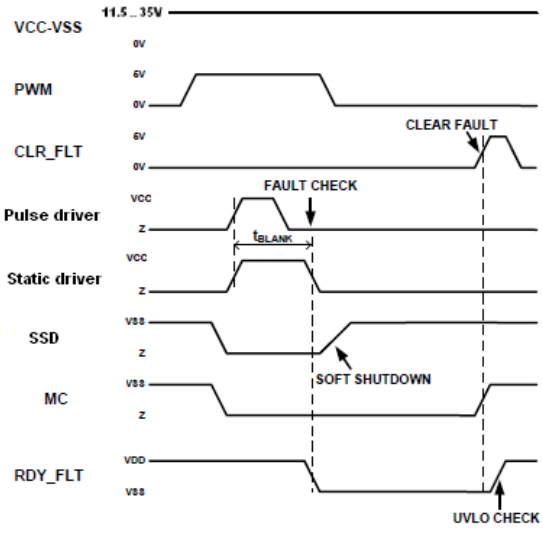
- When the PWM signal turns on, it is transferred after the propagation delay from the PWM inputs to the output Driver. During the pulse delay (about 220ns), the BASE is driven to 5.5V through a 1ohm resistor. After this delay, le BASE is driven to 5.5V through a 5ohm resistor until the PWM signal turns-off.
- When the PWM signal turns-off, the The BASE-EMITTER is discharge through an 1ohm resistor after the nonaverlaping delay after the propagation delay TOFF During the Miller Clamp delay (about 220ns). After the miller clamp delay, the Base is pulled directely to the VSS potential until the next PWM signal turns-on.

Fault phase

The faults considered when the PWM signal is high are :

- Desaturation detection on the COLLECTER terminal of the power transistor.
- Over-current detection on the BASE terminal of the power transistor.
- Over-current detection on the SOURCE terminal of the power transistor.

The UVLOs errors are checked permanently during the functional phase of the driver board, while the other failures are checked when the PWM signal is turned-on and outside the blanking time t_{BLANK} (about 1µs).
Immediately after fault detection, this information is sent to the microcontroller through the RDY_FLT signal by a "0". When the output driver is turned off, the Soft Shut-Down driver is turned on. This slowly turns-off the power transistor to avoid high dV/dt and high turn-off current.
In order to leave this state, a rising edge on CLR_FLT input signal is required. This also results in a new startup phase that starts immediately with no time-out.
It should be noted that the CLR_FLT input signal can be used as a reset pin for the drivers stage. Indeed, even when no fault is detected, a rising edge on CLR_FLT initializes a new startup phase.



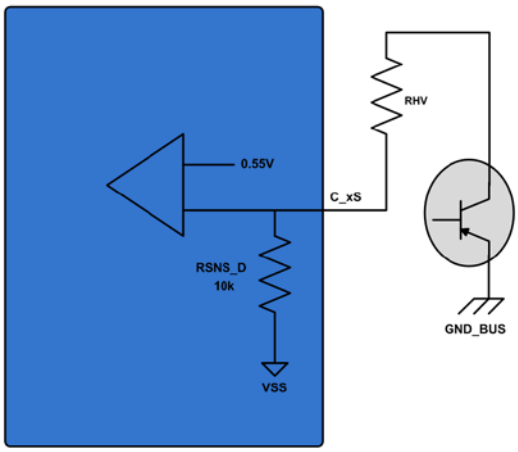
FUNCTIONAL FEATURES

Cross conduction protection

The cross conduction protection has been implemented to prevent short-circuiting the high voltage power supply through the High Side (HS) and Low Side (LS) power transistors of a half bridge. This is achieved through a bidirectional isolated data communication between the HS driver and the LS driver of the half bridge. The LS Driver is the master and the HS Driver is the slave. The input PWM signal of the board, is the same for HS driver and LS driver. The PWM LowSide signal is complemented at the LS transceiver stage.

Drain failure detection (desaturation)

When the power transistor is turned-on, the voltage on its collector must be very close to the voltage on its emitter. If this is not the case, a collector failure is detected using the circuit sketched below :



To simplify the equation for the computation of the desaturation threshold voltage V_{TH_DESAT}, we consider VSS=0V. The desatura-tion detection threshold V_{TH_DESAT} is then given by :

$$V_{TH\_DESAT} = \frac{R_{HV} + R_{SNS\_D}}{R_{SNS\_D}} \times 0.55V$$

The C_xS pin is internally clamped to 1.4V versus VSS pin with a maximum current sink of 5mA. The parasitic capacitors on this pin must be minimized as it's proportional to the current that can be tolerated in the resistor divider. This current must be high enough to quickly charge the parasitic capacitor. This charging time defines the desaturation detection delay after the blanking time. During the blanking time, the C_xS pin is forced to VSS to ensure no fault detection during the blanking time.

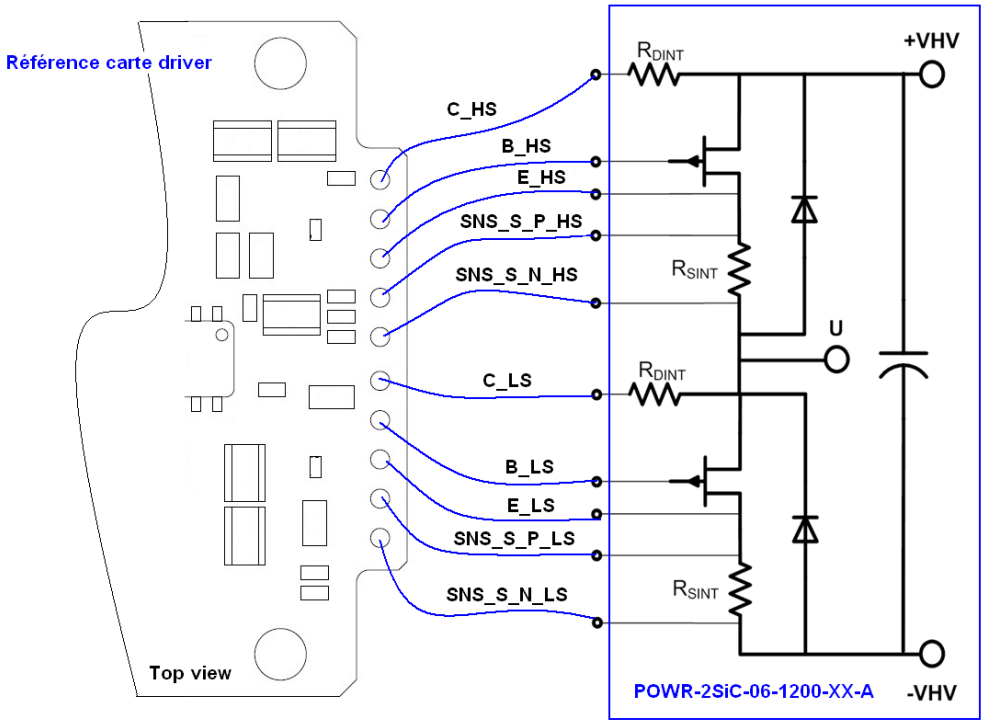
Source over-current detection

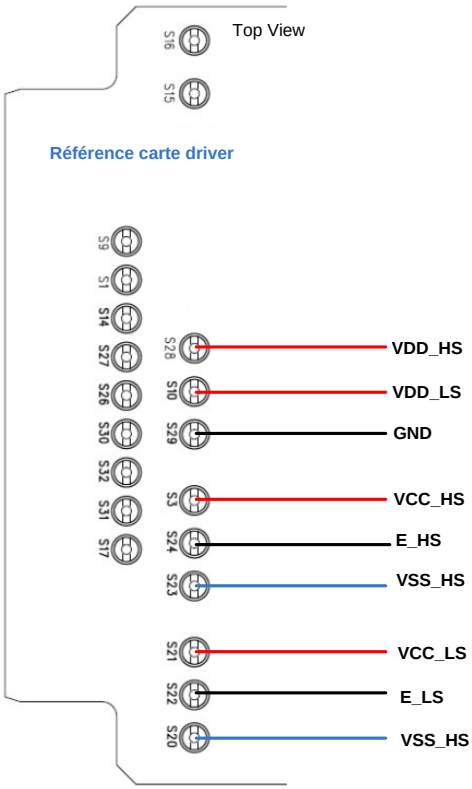
When the power transistor is turned-on, the source current is measured using the differential voltage between SNS_S_P_xS and SNS_S_N_xS and compared to a threshold fixed by the sense resistor R_{SNS_E}. In the case of damage on the emitter, the current should be higher than the fixed threshold indicating source failure for the circuit. The source over-current threshold is given by :

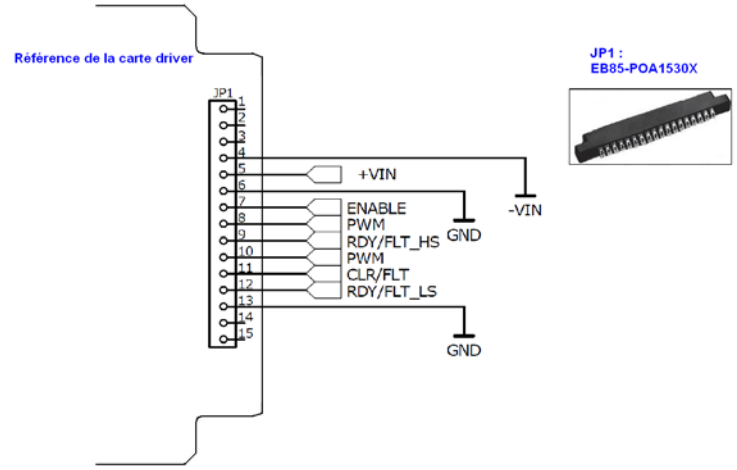
$$I_{TH\_E} = \frac{100mV}{R_{SNS\_E}}$$

For correct operation of the source over-current detection, a minimum voltage of 5V is need between GND_BUS and VSS. If for a given application this is not possible to fulfill, the over-current detection can be disabled by shorting both SNS_S_P and SNS_S_N to the E_xS potential.

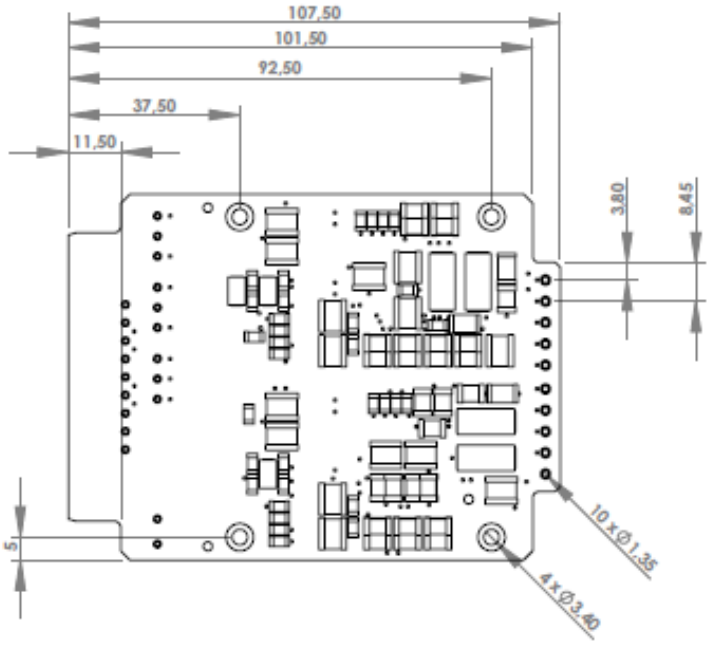
TYPICAL APPLICATION

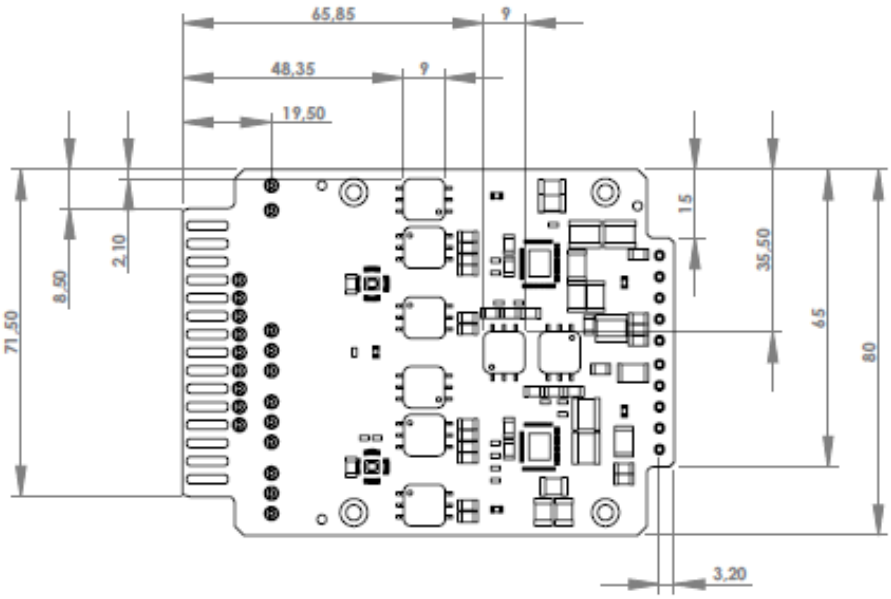






MECHANICAL DRAWING (Units in mm)





SOLDERING RECOMMANDATION

Hand Soldering is recommanded. All solder alloys should be compatible with the metalization finish noted on the mechanical characteristics pragraph. Solder tip temperature should be above 300°C and pre-heating is recommended for high melting point alloys. Module hermeticity allows dipping-like cleaning process.

ORDERING INFORMATION

DRIV	-	XXX	-	YYYY	-	01	-	A
Category		*Transistor Type*		*Switching Frequency*				
Driver Board		MOS: MosFET BJT: Bipolar Junction Transistor SJT: Super Junction Transistor HEM: High Electron Mobility Transistor		0100: 10kHz to 100kHz 0500: 100kHz to 500kHz 1000: 500kHz to 1MHz				